Novel Design Approach for X-Band GaAs Monolithic Analog 1/4 Frequency Divider

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Abstract—A novel analog frequency divider which can generate a 1/4 frequency component is proposed. The frequency divider consists of a dual-gate FET and a two-stage capacitor-resistor coupled amplifier. This circuit configuration also enables achieving a small-size GaAs MMIC analog frequency divider. In this analog frequency divider, the input signal f_0 is mixed with signal component f_0/x caused by noise or transients in a feedback loop. Then, a $(1-1/x)f_0$ IF component is induced and is again mixed with the input signal. This process delivers the f_0/x component regeneratively. Resultant continuous signal components f_0/x and $(1-1/x)f_0$ have a harmonic relation when the system reaches a steady state. The f_0/x component can be mainly obtained at an output port of the frequency divider. The operation band was simulated using a SPICE II computer program. The designed bandwidth and conversion gain for the 1/4 frequency divider are 8.5–10.6 GHz and −3 dB, respectively. Based on the simulation, a GaAs monolithic analog 1/4 frequency divider was made and tested. The developed 1/4 frequency divider provides a 8.5–10.2-GHz operation bandwidth and -5 ± 1-dB conversion gain. The designed and experimental values are in good agreement. The frequency division band can be shifted to higher frequency (10.65–11.2 GHz) by adopting the external matching circuit at the GaAs chip output port. The proposed analog frequency divider circuit can be applied not only for 1/4 frequency division, but also for $1/n$ frequency division (interger $n > 2$).

I. INTRODUCTION

HIGHER frequency stability is required for local oscillator sources used in microwave systems, communications, radar, and satellite broadcasting. A conventional method for achieving the requirement is to use GaAs FET oscillators stabilized by high-Q dielectric resonators, whose main compositions are titanium oxide and barium oxide.

However, this method has a disadvantage in that the resonators cannot be integrated monolithically. This becomes a serious drawback when mass production has to be taken into account. Recently, production demands for microwave frequency converters have increased rapidly, because 12-GHz band, direct satellite broadcasting services have been initiated. Realization of a fully monolithic, stabilized microwave local source is a key to achieving mass production.

A Phase Lock Loop (PLL) frequency stabilizing method, described in Fig. 1, enables full integration of microwave circuits. To realize the PLL method, monolithic frequency dividers operating at the X-band have to be newly developed.

Previously reported frequency dividers can be classified into three categories.

1) (*Digital Static*) Instantaneous frequency division is possible. Up to date performances reported at 7.5 GHz divide-by-four for a GaAs IC [1], 6.3 GHz divide-by-two for a AlGaAs/GaAs HEMT IC (300 K) [2], 8.6 GHz divide-by-four for a AlGaAs/GaAs HBT IC [3], and 9 GHz divide-by-eight for a Si bipolar IC [4].

2) (*Digital Dynamic*) Instantaneous frequency division is impossible. However, higher frequency operation than for digital static dividers can be achieved. Frequency division by two of 10.2 GHz has been reported [5].

3) (*Analog Regenerative*) The highest operation frequency is available in this category, in comparison with the other two. However, its bandwidth is comparatively narrow. Performance of a 16 GHz divide-by-two was reported in a GaAs FET hybrid IC construction [6]. At present, no Monolithic Microwave Integrated Circuits (MMIC) for the analog regenerative divider have been reported.

In the above-mentioned frequency dividers only the analog regenerative divider can be applied for microwave systems with sufficient operation margin. However, the conventional analog regenerative divider has two major disadvantages. First, it can be used only for 1/2 frequency division. In case of the DBS application (local oscillator frequency LO = 10.8 GHz), the 1/2 division component becomes 5.4 GHz, at which none of the commercially available IC's can operate. If a 1/4 division component (2.7 GHz) is realized, some commercially available IC's can be used in tandem with the frequency divider. Second, filtering circuits are very complicated and their sizes become too large to construct GaAs MMIC's. Therefore, the development of an analog $1/n$ (integer $n > 2$) frequency division technique with small circuit size is very important for microwave systems, especially for the DBS application.

In this paper, a novel analog 1/4 frequency divider, suitable for GaAs MMIC constructions, is proposed and its design and fabrication technique are described. The

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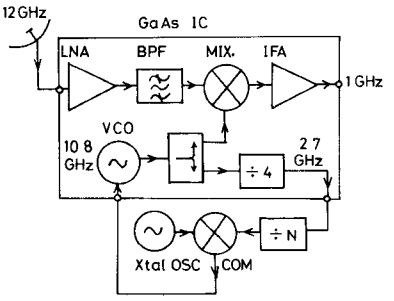


Fig. 1. Block diagram for microwave reception front end with PLL.

novel analog frequency divider consists of a switch and three inverters. With the developed GaAs monolithic analog frequency divider, 1/4 frequency division has been realized over the frequency range from 85. to 10.2 GHz (10.65–11.2 GHz: when an external matching circuit was added).

II. Operation Principle

Fig. 2 shows the operation principle for a conventional 1/2 analog regenerative frequency divider which involves a mixer, a bandpass filter ($f_0/2$), and an amplifier. A $f_0/2$ signal component, caused by noise or transients in the feedback loop, passes through the bandpass filter and is amplified. Then, the $f_0/2$ component is mixed with input signal (f_0) by the mixer. This process regenerates the $f_0/2$ component. Thus, the conventional analog regenerative frequency divider has been applied only for the 1/2 frequency division. Moreover, the circuit size for the bandpass filter becomes too large for fabricating GaAs MMIC's.

If the bandpass filter in Fig. 2 is removed, two signals f_1 and f_2, which satisfy (1), can exist in the feedback loop [7], [13]:

$$f_0 = f_1 + f_2. \tag{1}$$

The principle expressed by (1) is applied for newly developed GaAs monolithic analog frequency dividers.

Fig. 3 shows a block diagram for the newly developed frequency divider. In the figure, signal component f_0/x caused by noise or transients in the feedback loop, and the input signal (f_0) are mixed. Then, $(1 \pm 1/x)f_0$ IF components are induced. Only a lower side band of the IF signals passes through the low-pass filter and is again mixed with the input signal. This process delivers both $(2-1/x)f_0$ and f_0/x components. However, in the two signal components, only the f_0/x component can pass through the low-pass filter. Resultant continuous signal components in this system are f_0/x and $(1-1/x)f_0$.

If the system reaches a steady state, a harmonic relation exists between the two signals, because a waveform is represented by the Fourier series. Then,

$$\frac{1-\frac{1}{x}f_0}{f_0/x} = m \tag{2}$$

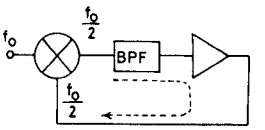


Fig. 2. Block diagram for conventional 1/2 analog regenerative frequency divider.

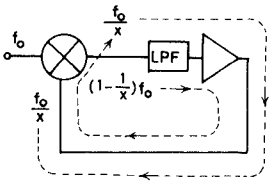


Fig. 3. Block diagram and operation principle for newly developed analog 1/4 regenerative frequency divider.

where m is an integer. From (2), x also becomes an integer

$$x = m+1. \tag{3}$$

To realize this operation, the feedback loop has to pass both signal components of $f_0(m+1)$ and $mf_0/(m+1)$. In addition, feedback loop gain at f_0 has to be suppressed to below unity to prevent undesirable oscillations. Therefore, cutoff frequency f_c for the low-pass filter is chosen as

$$\frac{mf_0}{m+1} < f_c < f_0. \tag{4}$$

Moreover, to get a large output for the $f_0/(m+1)$ component, the feedback loop has a natural frequency near $f_0/(m+1)$.

III. Design Example for 1/4 Frequency Divider

A. Natural Frequency

The block diagram shown in Fig. 3 is replaced by three inverters and one FET switch, as shown in Fig. 4. Assuming that the input signal is 10 GHz, a natural frequency near 2.5 GHz is required for a 1/4 frequency division. A ring oscillator, shown in Fig. 4, provides natural frequency f_r as

$$f_r \simeq \frac{1}{2(\tau_1+\tau_2+\tau_3)} \tag{5}$$

where $\tau_i (i=1,2,3)$ is a time delay for each inverter. As shown in Fig. 5, an inverter and an FET switch are nearly equivalent to a dual-gate FET. Then, an equivalent circuit for the newly developed GaAs monolithic analog frequency divider becomes as shown in Fig. 6.

In Fig. 6, T_1 and T_2 are matching circuit elements between the second gate of the dual-gate FET and the signal source. T_3 and T_4 perform as both peaking circuits and delay circuits, which adjust *fr*. The *fr* was simulated using the SPICE II program, where shallow gate-bias voltages are applied to cause a free-running oscillation. The simulated free-running oscillation, which gives f_r, was 2.656 GHz, as shown in Fig. 7.

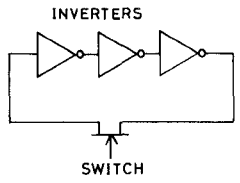


Fig. 4 Circuit diagram for newly developed analog 1/4 frequency divider.

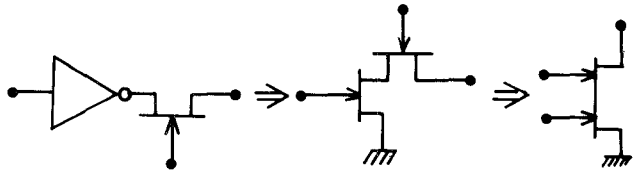


Fig. 5. Simplified model for dual-gate FET.

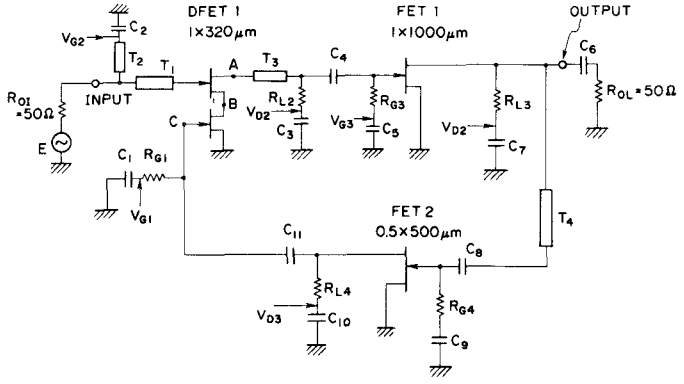


Fig. 6. Equivalent circuit for X-band GaAs monolithic 1/4 analog frequency divider.

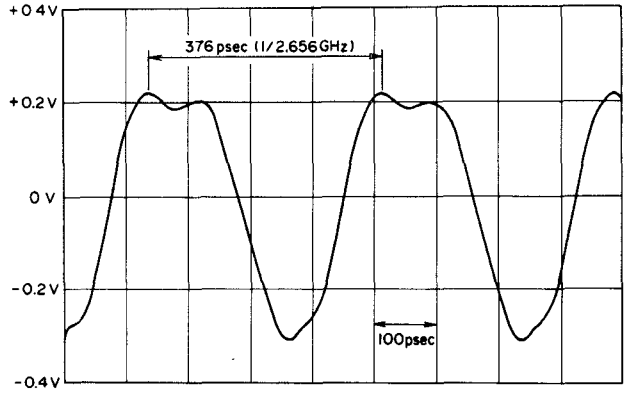


Fig. 7. Simulation for natural frequency using SPICE II program.

B. Open-Loop Gain

To estimate the feedback loop gain, open-loop voltage-gain $G_V = V_C/V_A$ was simulated, where the circuit is cut at both points A and B.

Point B is terminated to 50 Ω. V_A and V_C are voltages at points A and C, respectively. The simulation results are shown in Fig. 8. Large voltage gain was obtained around 2.5 GHz. At the frequencies near 7.5 GHz, more than a 0-dB gain was obtained. $|S_{21}|^2$ for the open circuit decreases monotonically. Since each FET has a load impedance consisting of the load resistor R_L and the next stage

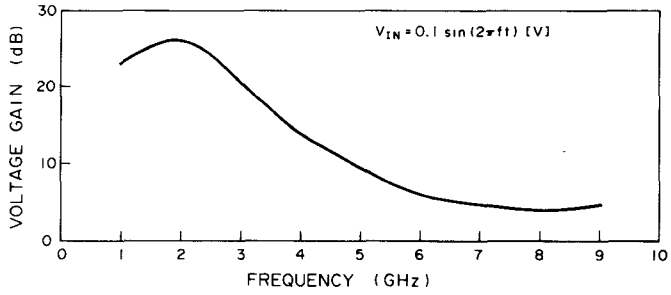


Fig. 8. Calculated open-loop voltage gain.

FET input capacitance C_{gs} in parallel, the inverter originally has low-pass filter characteristics. Input signal f_0 can be cut off without any filters. This configuration enables small circuit size. In Fig. 6, gate widths for FET1 and FET2 are chosen as 1000 and 500 μm, respectively, to achieve wider bandwidth [12].

C. Frequency Division

An output simulation waveform for 1/4 frequency division ($f_{in} = 10$ GHz, $f_{out} = 2.5$ GHz) is shown in Fig. 9. The bias-voltage condition is the same as in Fig. 8. As seen, there are harmonic (5 GHz, 7.5 GHz, 10 GHz) and subharmonic (1.25 GHz) frequency components due to the nonlinearity of the device. However, the main frequency component is 2.5 GHz, which corresponds to a 1/4 frequency component of the input signal.

Assuming that signal source voltage e is represented as

$$e = E_{10} \sin 2\pi ft \tag{7}$$

available input power P_{av} is written as follows:

$$P_{av} = \frac{E_{10}^2}{8R_{OI}}. \tag{8}$$

R_{OI} is the signal-source resistance.

On the other hand, output power P_L, which is dissipated at R_L is

$$P_L = \frac{E_{2.5}^2}{2R_{OL}} \tag{9}$$

where $E_{2.5}$ is the voltage amplitude for the 2.5 GHz output signal and R_{OL} is the load resistance. From (8) and (9), conversion-gain G_C(10 → 2.5 GHz) becomes

$$G_C = \frac{P_L}{P_{av}} = \frac{4R_{OI}}{R_{OL}} \left(\frac{E_{2.5}}{E_{10}} \right)^2. \tag{10}$$

In (10), substituting $R_{OL} = R_{OI} = 50$ Ω and $E_{10} \equiv 1$ V, $E_{2.5} \simeq 0.35$ V, G_C is calculated as -3 dB. A simulated bandwidth for 1/4 frequency division is 8.5–10.6 GHz. The simulated transient time to reach steady-state waveforms is about 2 nS (1/500 MHz). Since FM noise for local oscillators is mainly due to $1/f$ noise, which appears below several megahertz, a 2-nS response is sufficient for the PLL.

Fig. 10 shows an output waveform without free-running oscillation, where V_{G2} is deeply biased. The 1/4 frequency division is observed.

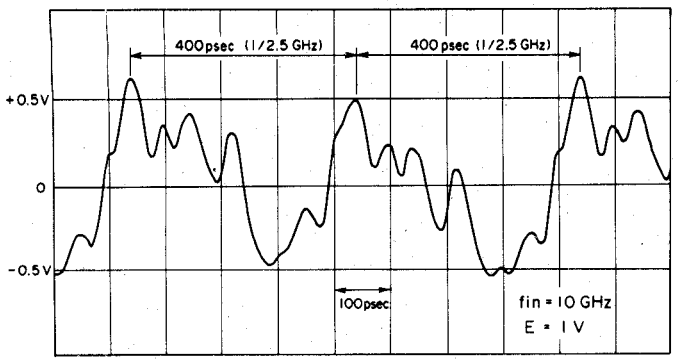


Fig. 9. Simulated output waveform for analog 1/4 frequency divider (f_{in} = 10 GHz, f_{out} = 2.5 GHz).

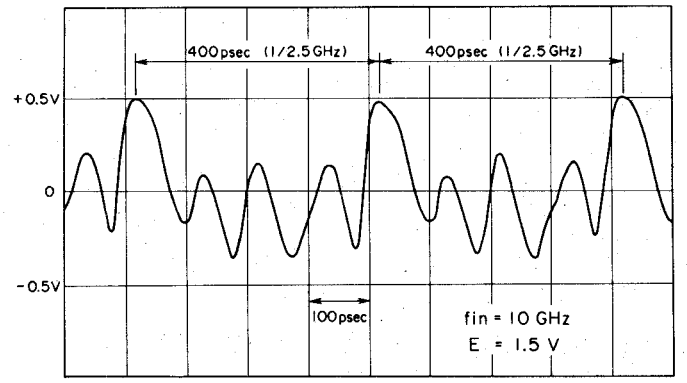


Fig. 10. Simulated output waveform for analog 1/4 frequency divider, where free-running oscillation without signal input is suppressed. (f_{in} = 10 GHz, f_{out} = 2.5 GHz.)

IV. Experimental Results

The equivalent circuit described in Fig. 6 was realized by using the GaAs MMIC technology. The process used is the ion-implanted closely spaced electrode FET process [10], [11], which has already been adopted for the *X*-band GaAs monolithic frequency converter [8] and the *X*-band GaAs monolithic voltage-controlled oscillators [9]. Fig. 11 shows a chip photograph for the newly developed GaAs monolithic analog frequency divider. Chip size is 1.8 mm × 1.3 mm × 150 μm. FET threshold voltage V_T is −1 V, transconductance g_{mo} is 150 mS/mm, and saturated drain-current I_{DSS} is 120 mA/mm. Load resistors are fabricated by using an ion-implanted n^+ layer, whose sheet resistivity is 130 Ω/□. Gate-bias voltage-supplying resistors are formed by the same layers as FET active layers. MIM capacitors are used and its insulator is CVD-SiO_2. A Ti–Pt–Au metal system is used for the capacitor top electrode and the microstrip conductor.

The GaAs monolithic frequency divider was mounted on a chip carrier and tested in a 50 Ω system. Measured f_r was 2.35 GHz. Fig. 12 shows a measured bandwidth for the 1/4 frequency division operation. Bias voltage conditions are $V_{G1} = -0.6$ V, $V_{G2} = -0.8$ V, $V_{G3} = -0.5$ V, $V_{G4} = -0.8$ V, $V_{D2} = 3$ V, $V_{D3} = 5.2$ V, and $V_{D4} = 6.1$ V. Under this condition, no free-running oscillation occurs. The vertical axis in Fig. 12 shows the minimum input power for the 1/4 frequency division operation. When the input power level is fixed at 10 dBm, the frequency division bandwidth is 8.5–10.2 GHz. When input power is increased to 14 dBm, the bandwidth becomes 8.25–10.4 GHz.

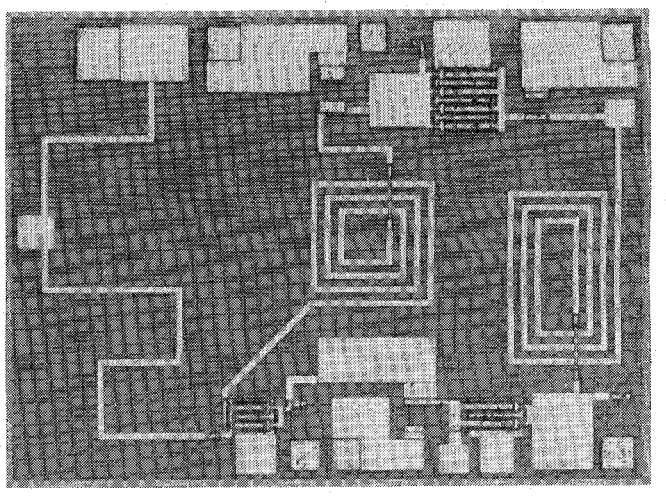


Fig. 11. Chip photograph for the newly developed GaAs monolithic analog frequency divider.

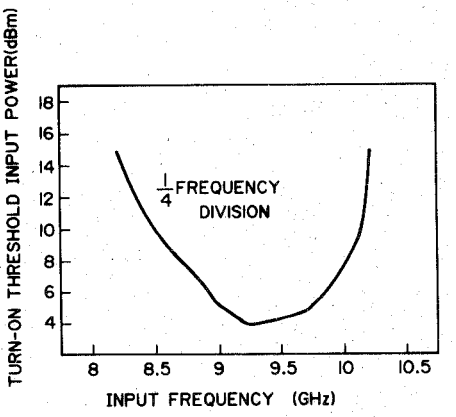


Fig. 12. Measured bandwidth for the GaAs monolithic analog frequency divider.

Fig. 13 shows measured input-output power conversion characteristics. Conversion gain for the 1/4 frequency division (10 GHz → 2.5 GHz) was -5 ± 1 dB over from the 4–12.5 dBm input power range. An 8-dBm power output was obtained at a 15-dBm power input. 5 and 7.5 GHz harmonic components were also observed. However, conversion gains for the harmonic components are very small. The power level for 5 GHz was 11 dB lower than for 2.5 GHz, as shown in Fig. 14, and the power level for 7.5 GHz (not shown in Fig. 13) was 24 dB lower than for 2.5 GHz. In addition, adopting a proper filter circuit after the frequency divider output port, undesirable frequency components can be greatly suppressed.

Fig. 14 shows output spectra for the frequency divider. Fig. 14(a) shows spectra for 1/4 frequency division, when input frequency is varied from 8.5–10.2 GHz, where input power is fixed at 10 dBm. The top and the bottom photographs show asynchronous spectra. The middle three photographs show synchronous spectra. In the f_{in} = 8.5–10.2-GHz frequency range, which corresponds to f_{out} =

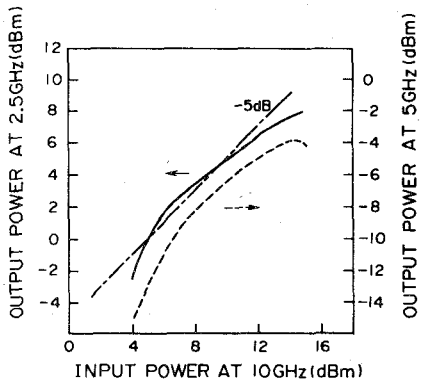
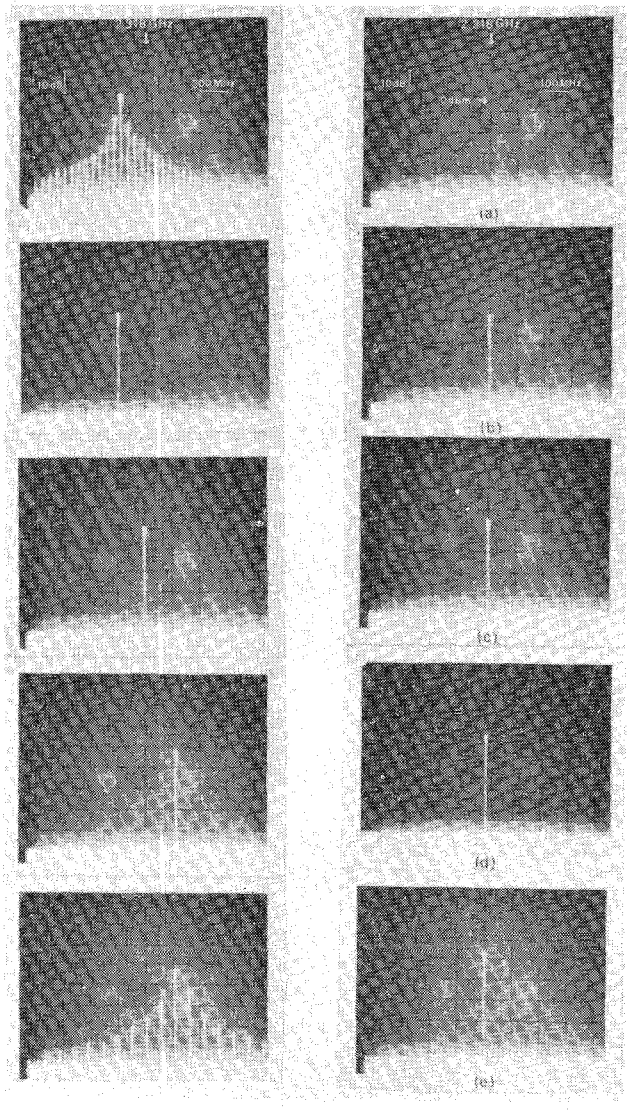


Fig. 13. Measured input–output power conversion characteristics for the GaAs monolithic frequency divider.



(a) (b)

Fig. 14. Output spectra for GaAs monolithic frequency divider. (a) Input frequency is varied from 8.5 to 10.2 GHz, where input power is fixed at 10 dBm. (b) Input power is varied from 3 to 15 dBm ((a) 3 dBm, (b) 4 dBm, (c) 5 dBm, (d) 10 dBm, (e) 15 dBm), where input frequency is fixed at 9.272 GHz.

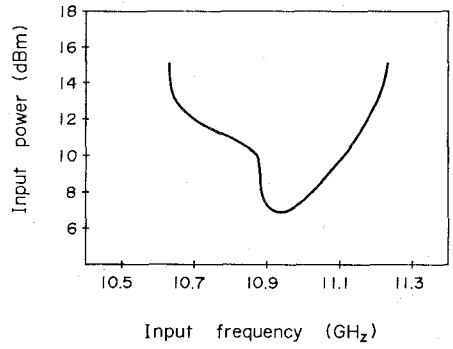


Fig. 15. Measured bandwidth with a reactive stub at the output port of the frequency divider chip.

2.125–2.550 GHz, synchronous spectra were observed. Fig. 14(b) shows the spectra for 1/4 frequency division, when input power is varied from 3 to 15 dBm, and input frequency is fixed at 9.272 GHz. Below 3-dBm power input, no signals and spurious oscillations were observed.

The operation band for the developed frequency divider can be changed by adopting an external matching circuit, because f_r and G_v are changed. Fig. 15 shows a measured bandwidth with a reactive stub at the output port of the GaAs chip. The band was shifted to higher frequency. From 10.65 to 11.2 GHz, 1/4 frequency division was observed, where input power is 15 dBm. In this case, conversion gain for 1/4 frequency division was -8 dB, that for 1/2 frequency division was -28 dB.

V. Conclusion

A novel analog frequency divider, which can generate a 1/4 frequency component, has been proposed. The frequency divider consists of a dual-gate FET and a two-stage capacitor-resistor coupled amplifier. This circuit configuration also enables achieving a small-size GaAs MMIC analog frequency divider. The operation band was simulated using a SPICE II computer program. The designed bandwidth and conversion gain for 1/4 frequency division are 8.5–10.6 GHz and -3 dB, respectively. Based on the simulation, a GaAs monolithic analog 1/4 frequency divider has been made and tested. The developed frequency divider provided a 8.5–10.2 GHz 1/4 frequency division range and -5 ± 1 dB conversion gain, which are in good agreement with the designed values. The frequency division bandwidth could be shifted to higher frequency (10.65–11.2 GHz) by adopting the external matching circuit at the GaAs chip output port.

The proposed analog frequency divider circuit can be applied not only for 1/4 frequency division, but also for $1/n$ frequency division (integer $n > 2$). In addition, the operation frequency range can be improved to higher frequencies in which active devices have power gains larger than unity. When using submicron gate length GaAs FET's or HEMT's as active devices, 30–40 GHz range frequency divisions are considered to be possible. The proposed analog frequency divider will be able to be used in microwave

and millimeter wave systems as the frequency divider for PLL-stabilized local sources.

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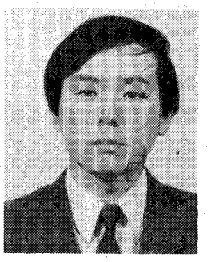

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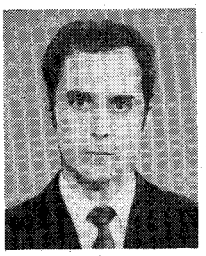

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